Notice of Allowability	Application No.	Applicant(s)	
	10/039,852	SHIH ET AL.	
	Examiner	Art Unit	
	John P. Trimmings	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment dated 2/17/2006*.

2. ☒ The allowed claim(s) is/are *1-3,5-9,10-11, renumbered as 1-9*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *03202006* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

DETAILED ACTION

This office action is in response to the applicant's amendment dated 2/17/2006.

The applicant has canceled Claims 4 and 9.

The applicant has amended Claims 1-3, 5-8 and 10.

Claims 1-3, 5-8 and 10-11 are pending.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Jiawei Huang on 3/16/2006.

The examiner and the applicant's representative, Jiawei Huang, agreed to amendments to Claims 1, 2 and 6 as follows:

Claim 1. (currently amended) A method of testing a chip that comprises ~~an~~ intellectual product circuit module<u>s</u>, the method comprising:

providing a test pattern;

sequentially enabling a common storage device to store the test pattern based on a plurality of different states; and

after the test pattern is stored in the common storage device, selecting one of the intellectual product circuit modules according to the test pattern for testing ~~and~~ <u>by</u> providing ~~the~~

a test activating signal ~~with~~ using a synchronous clock signal to the selected intellectual product circuit module~~s~~ in a next state, so that the selected intellectual product circuit module~~s~~ is operated and tested according to the test pattern from the common storage device.

Claim 2. (currently amended) A circuit for testing a chip that comprises an intellectual product circuit module, the circuit for testing the chip further comprising:

a common storage device coupled to the intellectual product circuit module; and

an input signal selector, coupled to the intellectual product circuit module and the common storage device, wherein

the input signal selector receives a test pattern and sequentially ~~enabling~~ enables the common storage device to store the test pattern based on a plurality of different states, after all of the test pattern is stored in the common storage device, in a next state the input selector further provides a test activating signal ~~with~~ using a synchronous clock signal to the intellectual product circuit module so that the intellectual product circuit module is operated and tested according to outputs of the common storage device.

Claim 6. (currently amended) A circuit for testing a chip that comprises a plurality of intellectual product circuit modules, the circuit comprising:

an output selector, coupled to the intellectual product circuit modules to selectively output a test result from the intellectual product circuit modules;

a common storage device, coupled to the intellectual product circuit modules to output signals stored in the common storage device to the intellectual product circuit modules; and

~~a~~ an input signal selector, coupled to the intellectual product circuit modules, the output selector and the common storage device, the input signal selector for receiving a test pattern

and sequentially enabling the common storage device to store the test pattern ~~base~~ based on a plurality of different states of the input signal selector, and after all of the test pattern is stored in the common storage device, selecting one of the intellectual product circuit modules according to the test pattern for testing ~~and~~ by providing a test activating signal ~~with~~ using a synchronous clock signal to the selected one of the intellectual product circuit modules in a next state, so that the selected intellectual circuit module is operated and tested according to the output of the common storage device, and the input signal selector further controlling the output selector to selectively output the test results.

Response to Amendments

2. In view of the applicant's amendments to Claims 1 and 6, the examiner withdraws the rejections of said claims under 35 USC 112 first paragraph.

3. In view of the applicant's amendments to the claims, and the examiner's amendments to Claims 1, 2 and 6, applicant's arguments, see Remarks, filed 2/17/2006, with respect to the rejection of Claims 1-11 under 35 USC 102(b), have been fully considered and are persuasive. The rejections of Claims 1-11 have been withdrawn.

Allowable Subject Matter

4. Claims 1-11 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: Couch teaches a circuit and method for testing a chip comprising intellectual

circuit modules, a common storage device, an input signal selector, selecting a module and testing said module. But the reference Couch, nor any other reference cited by the examiner, teaches or suggests the unique feature claimed by the applicant, wherein a synchronous clock pulse selects an intellectual circuit module to operate and test the module.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hancu, U.S. Patent No. 4945536.

Daniels et al., U.S. Patent No. 4860290.

Jaber, U.S. Patent No. 6028983.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2138

jpt

ALBERT DECADY
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